REMARKS

Claims 7-20 and 26-31 are pending. Claims 1-6 and 21-25 are hereby cancelled. Claims 7 and 13 have been amended and claims 26-31 are added to claim subject matter to which the Applicants are entitled. No new matter is added.

I. ELECTION/RESTRICTION

Applicant's have cancelled claims 1-6 and 21-25 in response to the Examiner's restriction.

II. DRAWING OBJECTION

The Examiner objected to the drawings for not including the reference sign "line 3-3" as described in the specification at page 5, lines 19-22. Applicants respectfully point out to the Examiner that "line 3-3" is not a reference number as defined by 37 CFR 1.84(p)(5). Rather, "line 3-3" represents a sectional view of a portion of Fig. 2 with regards to a thin film transistor memory cell before a write operation (Fig. 3A) and after a write operation (Fig. 3B). Therefore, Applicants respectfully request withdrawal of this objection.

III. CLAIM REJECTIONS

A. Claims 7-11, 13-16 and 20 are rejected under 35 U.S.C. § 103

The Office Action rejects claims 7-11, 13-16 and 20 under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 6,005,270 ("Noguchi") in view of U.S. Patent NO. 4,939,559 ("DiMaria"). Applicants respectfully traverse.

Noguchi discloses a thin film transistor memory device having charge storing layers. The charge storing layer has a function of holding a charge. When the charge is stored in the charge storing layer, an electric field is caused by the stored charge, therefore the threshold voltage of the memory transistor changes. See, Noguchi Patent, col. 2, lines 38-64.

By contrast, the present application discloses a thin transistor memory device having a physical conductive path, CP, that is formed where metal elements diffuse when a voltage is applied on the gate electrode. Noguchi fails to teach or suggest a conductive path. Rather, Noguchi contains charged storing layers to hold its charge, not a conductive path.

Furthermore, it is not obvious to someone of ordinary skill in the art to which said subject matter pertains to derive the present invention from Noguchi alone or in combination with DiMaria. Thus, Applicants respectfully request withdrawal of the rejection.

B. Claims 12 and 17 are rejected under 35 U.S.C. § 103

The Office Action rejects claims 12 and 17 under 35 U.S.C. § 103 as being unpatentable over Noguchi and DiMaria and further in view of U.S. Patent No. 5,644,528 ("Kojima"). Applicants' respectfully traverse.

With respect to claim 12, this claim is dependent on independent claim 7 and thus should be allowed for the reasons stated above for claim 7.

With respect to claim 17, this claim is dependent on independent claim 13 and thus should be allowed for the reasons stated above for claim 13.

C. Claims 18 and 19 are rejected under 35 U.S.C. § 103

The Office Action rejects claims 18 and 19 under 35 U.S.C. § 103 as being unpatentable over Noguchi and DiMaria and further in view of U.S. Patent No. 6,420,752 ("Ngo"). Applicant's respectfully traverse.

With respect to claims 18 and 19, these claims are dependent on independent claim 13 and thus should be allowed for the reasons stated above for claim 13.

CONCLUSION

In light of the above arguments, claims 7-20 and 26-31 are allowable over the references cited by the Examiner. Therefore, Applicants respectfully requests withdrawal of the outstanding rejections and a Notice of Allowance for the present application.

Attached hereto is a marked up version of the changes made to the claims by the current amendment. The attached pages are caption "**Version with Markings to Show Changes Made**". In addition, a clean copy of the pending claims is attached. The attached claims are captioned "**Pending Claims**".

If the Examiner believes that a telephonic or in-person interview would be helpful, he is invited and requested to call (202) 442-3000.

Respectfully submitted,

Date: **December 11, 2002**

Sean S. Wooden, Reg. No. 43,997
DORSEY & WHITNEY LLP
1001 Pennsylvania Ave
Suite 400 South
Washington, D.C. 20004
Fax (202) 442-3199
Voice (202) 442-3000

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Claims 1-6 and 21-25 have been canceled.

Claims 7 and 13 have been amended as follows:

7. (Amended) A memory cell, comprising:

a diffusive metal;

at least one floating gate;

a gate insulator disposed between the at least one floating gate and the diffusive metal, wherein the gate insulator includes a conductive path;

a channel region coupled to the gate insulator;

a source coupled to the channel region; and

a drain coupled to the channel region, wherein the diffusive metal is responsive to a write voltage to diffuse conductive elements through the gate insulator.

13. (Amended) A memory array, comprising:

a substrate;

a plurality of gate lines disposed over the substrate;

a plurality of data lines crossing the gate lines and disposed over the substrate; and

a plurality of memory cells at crossing points of the gate lines and data lines, each memory cell being coupled to a gate line and a data line that cross at the memory cell, wherein a memory cell comprises:

a diffusive metal;

at least one floating gate;

a gate insulator disposed between the at least one floating gate and the diffusive metal, wherein the gate insulator includes a conductive path;

a channel region coupled to the gate insulator;

a source coupled to the channel region; and

a drain coupled to the channel region, wherein the diffusive metal is responsive to a write voltage to diffuse conductive elements through the gate insulator.

Claims 26-31 have been added as follows:

26. (New) A memory cell, comprising:

a diffusive metal;

at least one floating gate;

a gate insulator disposed between the at least one floating gate and the diffusive metal, wherein the gate insulator includes a portion of the diffusive metal;

a channel region coupled to the gate insulator;

a source coupled to the channel region; and

a drain coupled to the channel region, wherein the diffusive metal is responsive to a write voltage to diffuse conductive elements through the gate insulator.

27. (New) The memory cell of claim 26, wherein the channel region, the source, and the drain are parts of a continuous layer of semiconductor material.

28. (New) The memory cell of claim 27, wherein the source and drain are doped regions of the layer of semiconductor material.

29. (New) The memory cell of claim 26, wherein the gate insulator extends between the diffusive metal and the floating gate, and between the floating gate and the channel region.

30. (New) The memory cell of claim 29, wherein the diffusive metal is a gate electrode.

31. (New) The memory cell of claim 26, wherein the at least one floating gate comprises a plurality of floating gates, the gate insulator extending between the floating gates.

PENDING CLAIMS

7. (Amended) A memory cell, comprising:

a diffusive metal;

at least one floating gate;

a gate insulator disposed between the at least one floating gate and the diffusive metal, wherein the gate insulator includes a conductive path;

a channel region coupled to the gate insulator;

a source coupled to the channel region; and

a drain coupled to the channel region, wherein the diffusive metal is responsive to a write voltage to diffuse conductive elements through the gate insulator.

8. The memory cell of claim 7, wherein the channel region, the source, and the drain are parts of a continuous layer of semiconductor material.

9. The memory cell of claim 8, wherein the source and drain are doped regions of the layer of semiconductor material.

10. The memory cell of claim 7, wherein the gate insulator extends between the diffusive metal and the floating gate, and between the floating gate and the channel region.

11. The memory cell of claim 10, wherein the diffusive metal is a gate electrode.

12. The memory cell of claim 7, wherein the at least one floating gate comprises a plurality of floating gates, the gate insulator extending between the floating gates.

13. (Amended) A memory array, comprising:

a substrate;

a plurality of gate lines disposed over the substrate;

a plurality of data lines crossing the gate lines and disposed over the substrate; and

a plurality of memory cells at crossing points of the gate lines and data lines, each memory cell being coupled to a gate line and a data line that cross at the memory cell, wherein a memory cell comprises:

a diffusive metal;

at least one floating gate;

a gate insulator disposed between the at least one floating gate and the diffusive metal, wherein the gate insulator includes a conductive path;

a channel region coupled to the gate insulator;

a source coupled to the channel region; and

a drain coupled to the channel region, wherein the diffusive metal is responsive to a write voltage to diffuse conductive elements through the gate insulator.

14. The memory array of claim 13, wherein the data lines comprise strips of semiconductor material, the sources and the drains comprising doped regions of the data lines.

15. The memory array of claim 13, wherein the gate insulator extends between the diffusive metal and the floating gate, and between the floating gate and the channel region.

16. The memory array of claim 13, wherein the gate lines are conductive lines coupled to the memory cells, the diffusive metal comprising a part of a gate line.

17. The memory array of claim 13, wherein the at least one floating gate comprises a plurality of floating gates, the gate insulator extending between the floating gates.

18. The memory array of claim 13, wherein the gate lines comprise:

a first conductor disposed over the gate insulator; and

a second conductor coupled to the first conductor.

19. The memory array of claim 18, wherein the first conductor includes a diffusive metal disposed between the insulator and the second conductor.

20. The memory array of claim 13, wherein the substrate comprises at least one of a glass or a plastic.

26. (New) A memory cell, comprising:

a diffusive metal;

at least one floating gate;

a gate insulator disposed between the at least one floating gate and the diffusive metal, wherein the gate insulator includes a portion of the diffusive metal;

a channel region coupled to the gate insulator;

a source coupled to the channel region; and

a drain coupled to the channel region, wherein the diffusive metal is responsive to a write voltage to diffuse conductive elements through the gate insulator.

27. (New) The memory cell of claim 26, wherein the channel region, the source, and the drain are parts of a continuous layer of semiconductor material.

28. (New) The memory cell of claim 27, wherein the source and drain are doped regions of the layer of semiconductor material.

29. (New) The memory cell of claim 26, wherein the gate insulator extends between the diffusive metal and the floating gate, and between the floating gate and the channel region.

30. (New) The memory cell of claim 29, wherein the diffusive metal is a gate electrode.

31. (New) The memory cell of claim 26, wherein the at least one floating gate comprises a plurality of floating gates, the gate insulator extending between the floating gates.